Unistep LabMaster Series

DFS

DIGITAL FREQUENCY SYNTHESIZER

USER MANUAL

V 1.2

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DFS ~~~ DFS DIGITAL FREQUENCY SYNTHESIZER ~~~

USER MANUAL

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1. INTRODUCTION

A short-wave HF frequency synthesizer circuit is at the heart of the DFS Module. The circuit is built around a VCO section controlled by a crystal oscillator, a prescaling divider, a PLL circuit, and a divide-by-n circuit. This circuit configuration is fundamentally identical to the ones used in all present-day frequency synthesized receivers and transmitters with digital tuners. Actual short-wave broadcast frequencies between the 120m – 11m bands can all be synthesized with the DFS circuit.

1.1 Features

- On-board oscillator and reference frequency generator
- Choice of two crystals for the master oscillator
- Provision for generating various reference frequencies
- VCO with excellent frequency linearity
- Frequency Synthesis between ~20 Hz - 25 MHz
- Low-Pass filtered output
- Socketed passive components for reconfiguring critical circuit parameters
- Full control of center frequency and PLL lock, capture, and other loop response properties
- Fully configurable divide-by-n counter
- Reverse polarity input power protection
- Fully socketed IC's for ease of repairs and maintenance

1.2 Package Contents

Please make sure that you have the following items in the ICL package:

1. The DFS Module (1)
2. User manual
3. Documentation CD

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2. CIRCUIT DESCRIPTION

2.1 Schematic Diagram

Full circuit diagram is included at the end of this manual. You may find it useful to keep it open while reading the following sections about the circuit details.

2.2 Circuit Operation

We can analyze the operation of the DFS circuit as several functional blocks:

- Reference Oscillator and Prescaler
- Phase Comparator
- VCO
- Divide-by-N Counter
- Power Input

Reference Oscillator and Prescaler

U1 IC works as the master oscillator and the first stage prescaler. To accommodate different sequence of frequency steps, two crystals are provided, selectable with the jumper block JMP2. The position of the shorting block on the JMP2 selects the crystal as follows:

JMP2 – 1	5.120 MHz
JMP2 – 2	4.096 MHz

The oscillator frequency selected by JMP2 is divided down to obtain the reference signal. A bank of jumper pins, JMP1, allows tapping the U1 divider chain at different points to obtain a reference signal of different frequencies as follows (The reference signal can be measured at TP3):

Shorting Jumper	Crystal Selected with JMP2 X1 (5.120 MHz)	X2 (4.096 MHz)
JMP1-1	20.00 kHz	16.00 kHz
JMP1-2	10.00 kHz	8.00 kHz
JMP1-3	5.00 kHz	4.00 kHz
JMP1-4	1.25 kHz	1.00 kHz
JMP1-5	0.625 kHz	0.500 kHz

Phase Comparator

Of the two phase comparators housed inside the U2 IC, only PC2 is used for the synthesis operation because it does not need a 50% duty cycle on the comparator input waveforms.

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Voltage-Controlled Oscillator

The VCO section of the PLL circuit is also housed inside the U2. Its input is connected to the PC2 output, after passing through the loop filter components.

The output of the VCO is taken to the J2 terminal block (J2-1) for external use and observation, as well as being fed back into the divide-by-n counter circuit.

The error signal that is internally used by the VCO circuit is also brought out as the demodulator signal (Dem) on U2-10 for observation and experimentation.

For more detailed investigation of the capabilities and operation of the U2 IC, please consult the datasheet included on the Documentation CD. Datasheet has extensive information on how this popular PLL device can be used in different applications.

The complete output terminal block, J2, assignments are as follows:

Terminal J2-1	Unfiltered output
Terminal J2-2	Low-pass filtered output
Terminal J2-3	Ground

Divide-By-N Circuit

At the core of the divide-by-n circuit is the fully configurable and very capable IC, U3. Using the S1, S2, and S3 DIP switches, U3 can be set to work as a divide-by-n counter across a very wide range. LED indicators connected to the DIP switches S1 and S2 provide a visible feedback while setting the divisor ratio.

Different operating modes for the U3 can be selected with the S2 DIP switch. Mode 5 seems to be useful for most common applications, so the DFS module comes with the DIP switch S3 set to "5". The U4 IC, along with the components around it provide a master reset to U3 for proper configuration setting.

For more detailed investigation of the capabilities and operation of the U3 IC, please consult the datasheet included on the Documentation CD. Datasheet has extensive information on the different modes of operation that is possible with this device.

Power Input

This is the circuit built around the Q1 Power MOSFET. It does two functions: **a)** Reverse power polarity protection with Q1 and R1, and **b)** Power supply filtering and decoupling with C1 and C2.

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3. FUNCTIONAL TESTING

The procedure included here can be used to make a quick but thorough check of all the circuit sections included on the DFS module.

Equipment required:

1. 40 MHz oscilloscope
2. 20 MHz frequency counter
3. 5 V DC power supply

Test Procedure

- ☐ 1. Apply power by connecting the power supply to the binding posts. D18 green LED should come on.
- ☐ 2. Measure the voltage at TP1. It should be about 40 mV less than the power supply voltage.
- ☐ 3. Make sure the jumper JMP1 is at position 3 and JMP2 is at position 1 and measure/observe the signal with a scope at TP2 for the presence of the 5.120 MHz oscillator output.
- ☐ 4. Change jumper JMP2 to position 2 and measure/observe the signal with a scope at TP2 for the presence of the 4.096 MHz oscillator output.
- ☐ 5. Change JP2 back to position 1 and measure the frequency of the signal at TP3. It should be 5.000 kHz.
- ☐ 6. Make sure the S1 and S2 DIP switch banks are set to their default positions as follows:

S1-1 to S1-7	OPEN (OFF)
S1-8	CLOSED (ON)

S2-1 to S2-5	OPEN (OFF)
S2-5	CLOSED (ON)
S2-7 to S2-8	OPEN (OFF)

- ☐ 7. Set S3 DIP switches as follows to set U3 to Divide-by-N Mode 5 :

S3-1	CLOSED (ON)
S3-2	OPEN (OFF)
S3-3	CLOSED (ON)
S3-4	Not Used

- ☐ 8. Measure the output signal at output terminal J2-1 and confirm that the frequency is 10.250 MHz.
- ☐ 9. Move the Jumper JMP1 to position 2 and confirm that the output is around 20.500 MHz.
- ☐ 10. Move JMP1 to position 4, and measure the output signal frequency. The output should be around 2.500 MHz. (Some frequency jitter is normal, since this frequency is just outside the lock range of the PLL with the components installed at the factory.)
- ☐ 11. Move JMP1 back to position 3, and set the S1 and S2 switches to all OFF except for the following:

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S1-7 CLOSED (ON)
S2-5 CLOSED (ON)

☐ 12. Measure the output frequency and make sure that it is 5.200 MHz.

If all the steps above check out, then you have a fairly healthy DFS module in your hands. Please do not forget to set all jumpers and DIP switches back to their default positions.

4. CHALLENGE COMPONENTS

If you have the DFS Challenge Module, you will notice that some components are not soldered to the PCB, but are instead mounted on single-pin sockets. These components are also marked on the schematic diagram with a dashed rectangular box around them. These components can be changed to modify circuit response characteristics.

These challenge components are the resistors and capacitors that determine the basic behaviour or response of their circuit sections. It is possible to modify the characteristics of these sections to new parameters by redesigning the circuit and replacing these components with different ones.

The design guidelines are included in the datasheets of the IC's, including some worked examples.

The single pin sockets have a good grip on the components leads for good electrical connection, so care should be taken while removing or inserting the challenge components. A good pair of long-nose pliers is almost a must while working with the challenge components.

5. APPLICATIONS

The primary design goal of the DFS circuit is frequency synthesis. By using the crystal oscillator and prescaler configuration jumpers, 10 different reference signals can be generated. Combined with the divide-by-n circuit divisor selection switches, DIP switches S1 and S2, frequency synthesis in a wide range with different step sizes is possible.

If desired, the loop filter and VCO circuits can be redesigned for different center frequency and PLL capture and lock characteristics.

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6. SPECIFICATIONS

Power Requirements	+5V DC @ 60 mA typical, 140 mA max.
VCO Range	20 Hz – 25 MHz typical with different components
PLL Capture Range	Same as VCO operation, with different components 3.0 MHz to 17 MHz as shipped from the factory
Dimensions	3.0”W x 4.0”L x 1.5”H

7. SUPPORT

We are here to help if you need assistance in using or troubleshooting the PLL Module. Please do not hesitate to contact Unistep Tech Support using any of the means listed below:

Internet Our web site www.unistep.ca has some support information and we are adding new material all the time.

E-Mail Please use our support address support@unistep.ca for any questions, comments, or recommendations you may wish to send our way.

Phone You can call us and leave a voice message to our support staff concerning any technical assistance you may need. We strive to return calls within one business day. You can find the contact phone number on the web site.

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